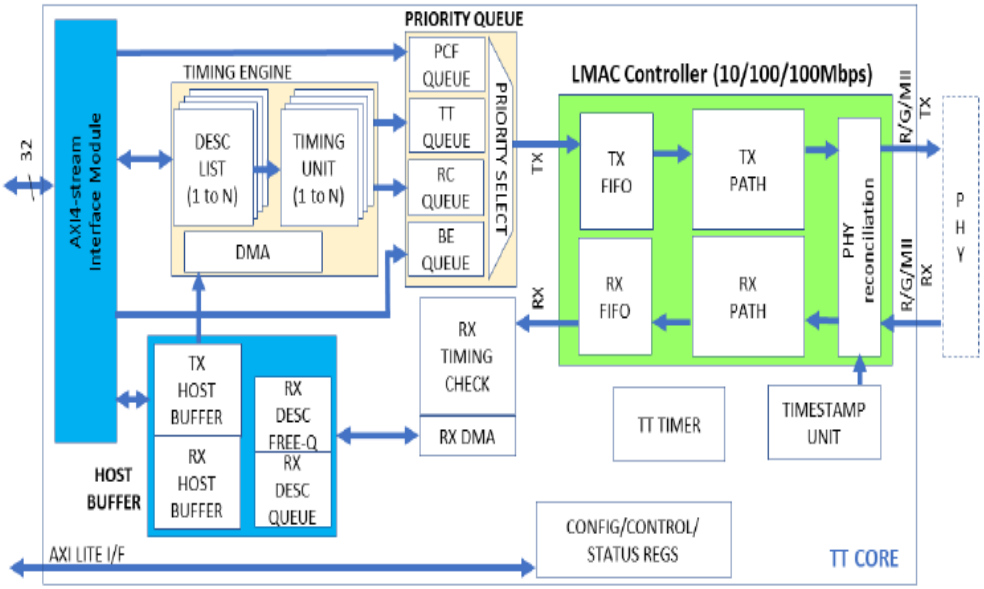
# Time Triggered Ethernet Core




## High Accuracy, Reliability, Fault Tolerant

- **Suitable for space and mission critical applications**
- **Conforms to Time-Triggered Ethernet SAE standard**
- **Well-known AXI Interface**
- **Configurable number of virtual links (streams)**

Time-triggered Ethernet (TTE) standard has been deployed in aircraft and spacecraft applications – well proven. From flight control to time-critical sensor applications, TTE is highly **versatile** and trusted to operate mission critical, high reliability applications including **aerospace**. TTE differs from regular Ethernet as it delivers data reliably and on-time – important for safety, deterministic applications. Organizations like NASA, ESA, Boeing, Airbus and others use TTE for their aerospace projects due to its ability to self-stabilize as well as help devices to maintain time synchronization and fault-tolerant (continue to function in the event of failure). TTE has been integrated in both civil and government aerospace systems. LeWiz has been working with customers to develop TTE technologies for use in aerospace. LeWiz TTE IP Core is a part of LeWiz comprehensive TTE solutions.

Using Time-Triggered Ethernet, the core performs time synchronization, time triggered traffic transmit and receive, and supports rate-controlled traffic/best-effort Ethernet traffic to provide users with reliable and fault-tolerant network. The core can be used for endpoint and switching systems. It has a configurable number of virtual links (VLs), each with a high timing accuracy, and monitors incoming traffic for meeting VL timing windows. The TTE core uses LeWiz Timing Engine which provides precision timing and had been production deployed in other time-critical applications.

For user interface, the TTE core provides an AXI-stream bridge and PHY interface. The AXI-stream bridge provides AXI-stream (AXIS) bus to connect to user internal bus. AXIS is well-known, fast and easy to use. The PHY interface facilitates a connection between the TTE core and external PHY via standard PHY protocols such as *GMII supporting up to 10Gbps or higher.

The TTE core is available with design examples, verification bench, documentation, and software. Due to the core's use of the common, well known standard protocols, the TTE Core is easy to integrate into the user's design environment and test. It can be licensed for designs, testing, production, and deployment.

# Time Triggered Ethernet Core

**FEATURES:**

- **Applicable for endpoint or switching systems**
- **Time sync protocol control frame (PCF) traffic handling without software assist for low latency**
- **Supports 4 traffic types on a network: PCF, time-triggered (TT), rate controlled, best effort**
- **Configurable number of virtual links**
- **Extensive tracking of TX/RX data, statistics and conditions – useful in network debug, optimization**
- **Verification bench: capable of using data from standard network tools or lab captured**
- **hardware timestamping**
- **64-bit AXI4 Stream for user bus interface**
- **Supports DMA to minimize CPU requirements**
- **Host and TT Core clocks can run at different frequencies – easy user meeting design timing**
- **ARINC 664-p7 compatible**
- **Applicable for FPGA or ASIC implementation**
- **Support deep nano-meter silicon process (12nm)**
- **Polling and interrupt mechanisms**
- **Hardware based packet transmission – accurate timing**
- **Fine grain timer with macrotick**
- **Independent priority queues**
- **Packet validity check**
- **Arrival window checking per virtual link**
- **1Gbps, 10Gbps, or higher**
- **Complete test bench**
- **Emulators available for easy development**
- **AXIS master emulator**
- **PHY/network emulator: Gbps PHY + network functions**

**AXIS TX Signals**
**(U = User; M = core module)**

| Signal | Direction | Description | |
|---|---|---|---|
| AXIS_Clk | U→ | User AXI bus clock<br>Activity can only occur on the rising edge of the clock. This clock can be different speed than the LMAC clock. | |
| **Main TX Bus** | | | |
| TX_AXIS_TDATA[N:0] | U→ | TX Stream Data bus<br>N = 31 for this 32-bit implementation<br>(Options for higher performing Ethernet speed of 10Gbps (N = 63) and 100Gbps (N = 255) are also available.) | |
| TX_AXIS_TSTRB[K:0] | U→ | TX bus strobe. Drives out along with the TDATA bus.<br>1 strobe bit for each 8-bit lane. If the strobe bit is<br>1, it means data is available on the lane.<br>Strobe 0 = lane 0 = [7:0]<br>Strobe 1 = lane 1 = [15:8]<br>Strobe 2 = lane 2 = [23:16]<br>Etc. | |
| TX_AXIS_TVALID | U→ | TX bus valid<br>Must be 1 for each valid data beat on the data bus.<br>If not valid (i.e. 0), both the TSTRB and TDATA must be ignored. | |
| TX_AXIS_TLAST | U→ | TX bus last beat indicator<br>Must be 1 for the last valid data beat on the data bus. | |
| TX_AXIS_TREADY | ←M | TX bus is ready to receive the data<br>When this is 1, the TT Core is ready to receive a full packet of 1500 data bytes. A packet must be streaming into the TT Core in a single burst, i.e., no gap between data beats.<br>If 0, it means the TT Core FIFO is full and cannot receive more transmit data. | |
| TX_AXIS_TUSER | U→ | TX bus error indicator. Reserved signal.<br>(Not used. User logic should qualify its data before sending to the TT Core and should not send bad data into the TT Core.) | |

The following shows the signals of the AXIS receive bus.

| Signal | Direction | Description | |
|---|---|---|---|
| AXIS_Clk | U→ | User AXI bus clock<br>Activity can only occur on the rising edge of the clock. This clock can be different speed than the LMAC clock. The TX and RX stream interfaces share a clock. | |
| **Main TX Bus** | | | |
| RX_AXIS_TDATA[N:0] | ←M | RX Stream Data bus<br>N = 31 for this implementation | |
| RX_AXIS_TSTRB[K:0] | ←M | RX bus strobe. Drives out along with the TDATA bus.<br>1 strobe bit for each 8-bit lane. If the strobe bit is<br>1, it means data is available on the lane.<br>Strobe 0 = lane 0 = [7:0]<br>Strobe 1 = lane 1 = [15:8]<br>Strobe 2 = lane 2 = [23:16]<br>Etc. | |
| RX_AXIS_TVALID | ←M | RX bus valid<br>Must be 1 for each valid data beat on the data bus.<br>If not valid (i.e. 0), both the TSTRB and TDATA must be ignored.<br>If the user logic is READY, it must be able to accept continuous data of a packet, i.e., TT Core will stream the packet out in a single burst. | |
| RX_AXIS_TLAST | ←M | RX bus last data beat indicator<br>Must be 1 for the last valid data beat on the TDATA bus. | |
| RX_AXIS_TREADY | U→ | User RX bus is ready to receive the data<br>(This signal is used in conjunction with the COMPATIBLE_MODE side band signal on the LMAC. If COMPATIBLE_MODE = 1, the LMAC always assume the user logic is ready to receive the data. This is similar to MAC controllers from FPGA devices.<br>COMPATIBLE_MODE = 1 is the only mode supported.<br>Wait state between the TDATA beats during the data transfer is not supported.) | |
| RX_AXIS_TUSER | ←M | RX bus error indicator.<br>Used by the LMAC to indicate error condition has been detected on the received Ethernet packet. | |



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