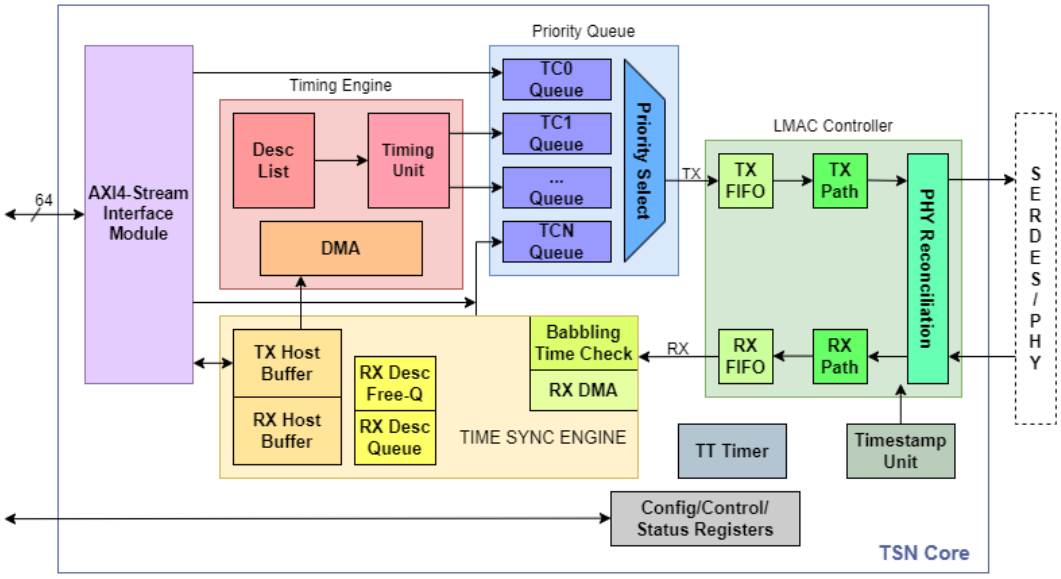
Time Sensitive Network IP Core

Fault Tolerant and Precise



- **Scalable from 1Gbps to 10Gbps**
- **Babbling Protection and Anti-Masquerading fault tolerant functions**
- **AXI standard – easy user interface hardware and software**

Standard Ethernet network equipment lacks concept of time, deterministic and guaranteed timely delivery. Time-Sensitive Networking (TSN), a set of standards for commercial and aerospace under the development of the IEEE and SAE organizations, defined the abilities for time synchronization, scheduling and traffic shaping, selection of communication paths, path reservations, and fault tolerance.

There are many TSN standard specifications. In aerospace applications, IEEE Std 802.1AS and 802.1IDP standards are of particular interest. TSN has similarities to its predecessor, time-triggered Ethernet (TTE), in capabilities and features, but TSN has wider support. It uses the well-known Precision Time Protocol (PTP) and the standards are developed in conjunction with many organizations from commercial and government sectors. It's expected to be used in industrial automation, automotive, aerospace, medical, and others – potentially having wide adoption.

Previously, LeWiz developed a precision, multi-speed TTE Core for endpoint and switching applications. With this IP core offer, we provide solutions for TSN supporting endpoint, switches and other user equipment. The technology can be used in FPGA, ASIC, and SoC devices and includes software support, simulation bench, documentation, etc.

The TSN IP core is designed to be scalable from 1Gbps to 10Gbps or higher, suitable for use in high reliability aerospace applications. The core mainly consists of an Ethernet front-end media access controller (MAC), a timing engine, Time-sync engine, and host interface unit for high speed, low latency data movements. The MAC is the LeWiz LMAC Core2 with 10/5/2.5/1Gbps speeds and the flexible PHY interface supports X/R/G/MII standards, compatible with various PHY and SerDes designs on or off chip. It has a register control unit to that allows software to configure the core and network functions. This unit uses the well-known AXI-lite bus.

The core's AXI* interface module allows it to operate at a different frequency than the host clock's speed. For example, the AXIS bus may be running at a clock frequency relative to the on-chip processor or internal bus while the core's internal clock may be running relative to the Ethernet PHY speed.

The fine grain on-chip timer provides time in microticks and macroticks for users to track time. Its frequency can be a function of the global clock or a dedicated clock which can be supplied from an ultra-accurate source, i.e., does not drift over voltage or temperature variation so that the clock remains stable.

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TSN IP Core

Its priority queue supports multi-level priority traffic classes required by the TSN standards. Utilization of the priority queue is application dependant and controllable by software.

LeWiz TSN IP Core supports multiple traffic types including PTP or time-sync, time-critical (TSN), rate controlled, and best effort (or normal Ethernet) traffic. An on-chip hardware engine supports time sync for precision and low-latency and works in master or slave mode supporting 1-step and 2-step time sync functions.

The core supports 3-plane network for fault tolerance. It's capable of handling babbling and other mal conditions in the network. It supports a space-capable version suitable for low-Earth orbit, deep space, and others. The fault tolerant capability enables the device to continue to function even when encountering errors due to radiation and other severe conditions in space applications.

There is also a verification bench; this bench is composed of 3 major units: the master emulator, device under test, and PHY/network emulator. The master emulator generates data or packets that are sent to the core under test or TSN Core. The packets can be hardcoded by users or previously captured by the user and embedded into the master emulator. The bench is useful for debugging in user-friendly simulation environments with real data/conditions found during field deployment.

FEATURES:

- Supports FPGA, ASIC, and SoC technology
- Supports 10G/5G/2.5G/1Gbps speeds
- Compatible with aerospace standard(s)
- Supports TSN network master or slave mode
- LeWiz provides solutions for both TSN or TTE network
- Well-known AXI-stream bridge for user logic interfacing – easy integration
- Host interface unit that provides high speed, low latency data movements
- Extensive statistic counters tracking data and conditions transferred or received
- PHY interface compatible with several PHY and SerDes designs, supports X/R/G/MII standards
- Configurable internal clock and timing clock – software control and adjustable
- TSN Core's internal logic can operate at a different frequency than the host clock speed – easy integration
- On-chip timer – time tracking for both microticks and macroticks
- Multi-level priority traffic, priority queue
- Supporting all traffic classes required by TSN
- Compatible with ARINC664-p7 standard
- Accurate timestamping
- Prevents babbling and masquerading
- 3-plane fault tolerant
- Verification bench for debugging
- Example design and verification scripts
- Space capable version

Interface signals:

Signal	Direction	Description
AXIS_Clk	U→	User AXI bus clock Activity can only occur on the rising edge of the clock. This clock can be different speed than the LMAC clock.
		Main TX Bus
TX_AXIS_TDATA[N:0]	U→	TX Stream Data bus N = 31 for this 32-bit implementation (Options for higher performing Ethernet speed of 10Gbps (N = 63) and 100Gbps (N = 255) are also available.)
TX_AXIS_TSTRB[K:0]	U→	TX bus strobe. Drives out along with the TDATA bus. 1 strobe bit for each 8-bit lane. If the strobe bit is 1, it means data is available on the lane. Strobe 0 = lane 0 = [7:0] Strobe 1 = lane 1 = [15:8] Strobe 2 = lane 2 = [23:16] Etc.
TX_AXIS_TVALID	U→	TX bus valid Must be 1 for each valid data beat on the data bus. If not valid (i.e. 0), both the TSTRB and TDATA must be ignored.
TX_AXIS_TLAST	U→	TX bus last beat indicator Must be 1 for the last valid data beat on the data bus.
TX_AXIS_TREADY	←M	TX bus is ready to receive the data When this is 1, the TT Core is ready to receive a full packet of 1500 data bytes. A packet must be streaming into the TT Core in a single burst, i.e., no gap between data beats. If 0, it means the TT Core FIFO is full and cannot receive more transmit data.
TX_AXIS_TUSER	U→	TX bus error indicator. Reserved signal. (Not used. User logic should qualify its data before sending to the TT Core and should not send bad data into the TT Core.)

Figure 1: AXIS Tx Signals

Signal	Direction	Description
AXIS_Clk	U→	User AXI bus clock Activity can only occur on the rising edge of the clock. This clock can be different speed than the LMAC clock. The TX and RX stream interfaces share a clock.
		Main TX Bus
RX_AXIS_TDATA[N:0]	←M	RX Stream Data bus N = 31 for this implementation
RX_AXIS_TSTRB[K:0]	←M	RX bus strobe. Drives out along with the TDATA bus. 1 strobe bit for each 8-bit lane. If the strobe bit is 1, it means data is available on the lane. Strobe 0 = lane 0 = [7:0] Strobe 1 = lane 1 = [15:8] Strobe 2 = lane 2 = [23:16] Etc.
RX_AXIS_TVALID	←M	RX bus valid Must be 1 for each valid data beat on the data bus. If not valid (i.e. 0), both the TSTRB and TDATA must be ignored. If the user logic is READY, it must be able to accept continuous data of a packet, i.e., TT Core will stream the packet out in a single burst.
RX_AXIS_TLAST	←M	RX bus last data beat indicator Must be 1 for the last valid data beat on the TDATA bus.
RX_AXIS_TREADY	U→	User RX bus is ready to receive the data (This signal is used in conjunction with the COMPATIBLE_MODE side band signal on the LMAC. If COMPATIBLE_MODE = 1, the LMAC always assume the user logic is ready to receive the data. This is similar to MAC controllers from FPGA devices. COMPATIBLE_MODE = 1 is the only mode supported. Wait state between the TDATA beats during the data transfer is not supported.)
RX_AXIS_TUSER	←M	RX bus error indicator. Used by the LMAC to indicate error condition has been detected on the received Ethernet packet.

Figure 2: AXIS Rx signals

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