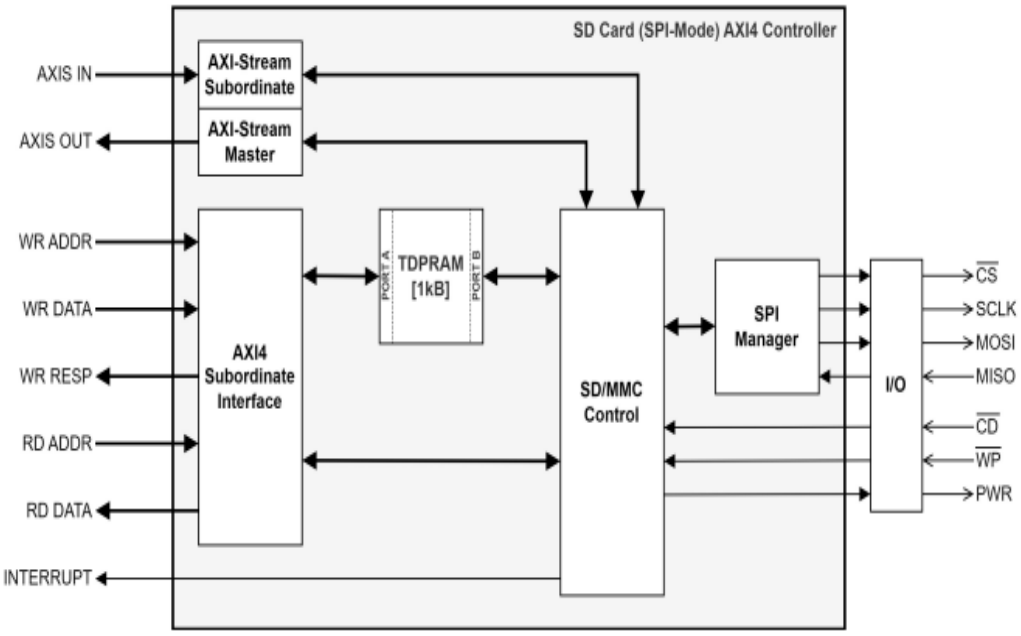
SD Card Controller Core



FAST AND EFFICIENT

- **Support 3 types of SD/MCC cards**
- **Block based Read/Write**
- **Designed for FPGA or ASIC**
- **Support SPI mode**
- **Interface: AXI4 or AXI stream**

SD cards, especially the micro types, are used in many applications for storing programs, configuration data, tables, or used as external storage device. SD Controller core uses the System Peripheral Interface (SPI) to communicate with the SD-card in electronic systems. SPI is a very well-known serial communication bus. It uses few signals and does not require specialized transceivers which is an advantage for ASIC designs. **Chips** (whether ASIC or FPGA) can integrate LeWiz SD controller(s) for connecting to **external SD-card, flash memory, and other peripherals**. Other uses of LeWiz SD Controller core include read/write of **stored bit files for FPGA configuration** as well as **software** programs/data for SOC chips that are used in applications such as aerospace, storage systems, network control, etc.

Designed for **short-distance** inter-chip communication, the SD controller core excels in **data transfers to/from SD cards** and from external SPI device(s). Additionally, through the device's master-slave interface, the SD controller core has **efficient data transmissions** with on-chip buffers. A single controller can **simultaneously** manage **multiple slave peripheral devices**.

FEATURES:

- Connects and manages of data transfers to and from SD cards and multimedia cards
- Built-in support for SD card booting, read/write functions, and others
- Supports different types of SD card response formats
- Easy command – response mechanism
- Uses SPI for reduced pin count and standard interface signaling
- On-chip buffers for continuous data streaming and high data transfer rate
- Single and multi block read/write capabilities
- Supports AXI4 protocol for on-chip interfacing → multiple, pipelined data transfers
- Also supports AXI-stream protocol for on-chip interfacing – flexible to adapt to user on-chip environment
- Prioritizes efficiency and latency
- Supports **SD and MMC** card types (multiple versions)
- Supports SD cards from many different manufacturers
- Supports interrupt or polling mechanisms

SPI Controller Module

- **Validated on Xilinx FPGA platforms**
- Licensable in source or netlist format
- (option) Available as space flight capable core

Interface signals:

Signal	Source	Description
ACLK	Clock	Global clock signal.
ARESETn	Reset	Global reset signal, active LOW.

Figure 1: AXI4 global signals

Signal	Source	Width	Description
AWID	Master	8	Write address ID. Tag for the write address group.
AWADDR	Master	64	Write address. Address for the first transfer.
AWLEN	Master	8	Burst length. Number of transfers within burst.
AWSIZE	Master	3	Burst size for each transfer.
AWBURST	Master	2	Burst type. Fixed (0b'00), Incrementing (0'b01), & Wrapping (0'b10).
AWVALID	Master	1	Write address valid.
AWREADY	Sub.	1	Write address ready.

Figure 2: AXI4 Write Address channel busses

Signal	Source	Width	Description
WDATA	Master	64	Write data.
WSTRB	Master	8	Write strobe. Each strobe bit indicates a byte of valid data.
WLAST	Master	1	Write last. Indicates last transfer.
WVALID	Master	1	Write data valid.
WREADY	Sub.	1	Write data ready.

Figure 3: AXI4 Write Data channel busses

Signal	Source	Width	Description
BID	Sub.	8	Write ID tag.
BRESP	Sub.	2	Write response. 2-bit Encoded signal.
BVALID	Sub.	1	Write response valid.
BREADY	Master	1	Write response ready.

Figure 4: AXI4 write response channel signals

Signal	Source	Width	Description
ARID	Master	8	Read address ID. Tag for the read address group.
ARADDR	Master	64	Read address. Address for the first transfer.
ARLEN	Master	8	Burst length. Number of transfers within burst.
ARSIZE	Master	3	Burst size for each transfer.
ARBURST	Master	2	Burst type. Fixed (0b'00), Incrementing (0'b01), & Wrapping (0'b10).
ARVALID	Master	1	Read address valid.
ARREADY	Sub.	1	Read address ready.

Figure 5: AXI4 Read Address channel busses

Signal	Source	Width	Description
RID	Sub.	8	Read ID tag.
RDATA	Sub.	64	Read data.
RRESP	Sub.	2	Read response. 4-bit encoded signal.
RLAST	Sub.	1	Read last. Indicates last transfer.
RVALID	Sub.	1	Read data valid.
RREADY	Master	1	Read data ready.

Figure 6: AXI4 Read Data channel busses

Signal	Source	Description
CLOCK	Clock	The global clock signal.
ARESETn	Reset	The global reset signal.
TVALID	Transmitter	Indicates the transmitter is driving a valid signal.
TREADY	Receiver	Indicates the receiver can accept a transfer.
TDATA	Transmitter	The data bus.
TKEEP	Transmitter	Indicates bytes of TDATA that are processed as part of the data stream.
TLAST	Transmitter	Indicates boundary of a packet.

Figure 7: AXI-Stream channel signals

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