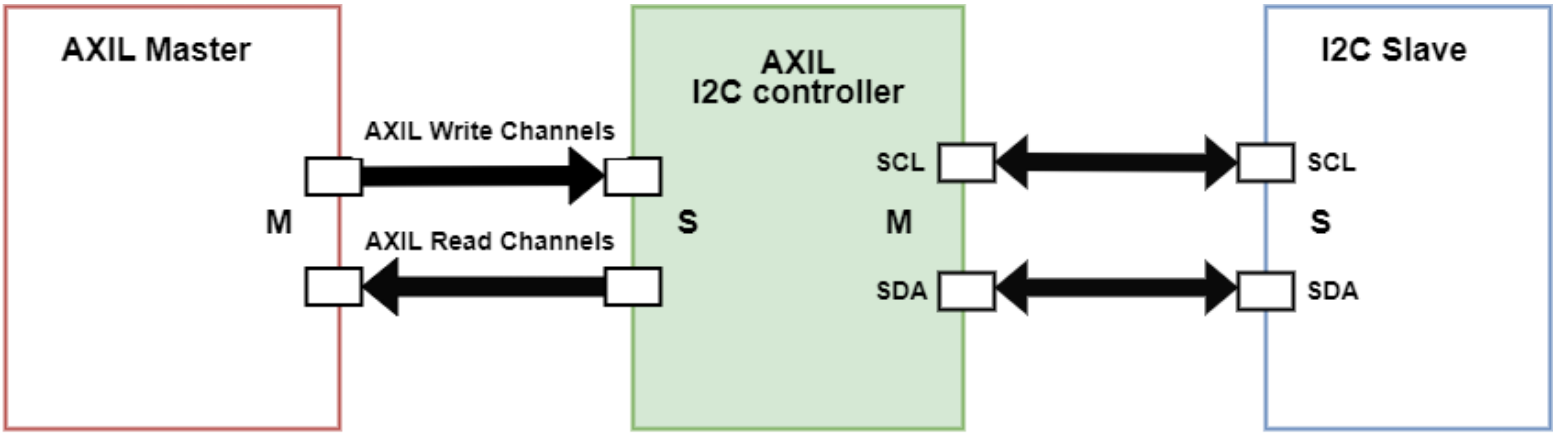
AXI-Lite I2C Controller Core

Simple, Easy to Use I2C Controller



M : Master S : Slave

- **32b AXI-Lite Interface**
- **Simple, register based I2C communication**
- **Designed for FPGA and ASIC**

Inter-Integrated Circuit or I2C is a widely used protocol, popular for bidirectional communication between master and low speed peripherals. The I2C interface allows for bi-directional communication with multiple slave devices from a master device. Its advantages include low-power and require very few pins – 2 pins. Its interface is integrated into many sensors such as temperature sensors, accelerometers, gyroscopes, fans, bridging chips, EEPROMs, flash memory, FPGAs, CPLDs, GPIO expanders and many more.

LeWiz AXI-Lite I2C Controller (Controller) incorporates I2C interface for connecting to the I2C slave devices. It has a 32-bit AXI-Lite (AXIL) interface to facilitate communication between the AXIL bus master and the AXIL I2C Controller. Control of the AXIL I2C Controller is via its registers – simple for software to use.

Its registers are used for functions such as holding configuration/control, status information and necessary for data exchange. The registers are each 32-bits wide and divided into 4 groups:

The Write Data Register Group holds written data (up to 8 bytes) from the AXIL interface that is eventually used for transmitting out of the I2C bus by the Controller. This group has 2 registers to contain the upper and lower 32 bits of the transmitting data. Software writes to these registers for transmitting data out.

The Read Data Register Group holds the data read from the external I2C device (up to 8 bytes per read). There are 2 32-bit registers holding the upper and lower parts of the up-to-8-byte data. Software read out the data from these registers for each I2C cycle.

The Write/Read Address/Control Register Group contains the I2C device address, write/read cycle control information. It also contains the status of the I2C operations and specifies the number of data bytes performed.

AXI-Lite I2C Controller Core

The Time Related Group defines timing characters of the I2C operations including controlling timings of the SCL and SDA signals as well as the frequency and duty cycle of the SCL clock signal.

The Controller core is available. It also has a test bench, test vectors, documents, design examples, and space-capable version. The I2C core can be integrated in user design environment through AXIL bus. AXIL is well known and simple to use.

FEATURES:

- Uses simple AXI-Lite Interface – VALID/READY handshake mechanism
- Facilitates communication between AXIL bus master and I2C slave device(s)
- Supports simple single transfer – up to 8 bytes per transfer
- 16 registers (32 bits wide, divided into 4 groups)
- Simple control, status, data mechanism
- Efficient address decoding, state machine control, and data buffering
- Bidirectional I2C bus
- Can be used with FPGA or ASIC development
- Compatibility with a wide range of I2C devices and simulation models.
- Available for rad-hard applications

Interface signals:

Table 1: Write Address Channel Signals.

Signal Name	Width	Source	Description
AWVALID	1’b0	Master	Indicates that the address and control information are valid and can be read by the slave.
AWREADY	1’b0	Slave	Indicates that the slave is ready to accept the address and control information
AWADDR	32’b0	Master	The write address where data is to be written

Table2: Write Data Channel Signals.

Signal Name	Width	Source	Description
WVALID	1’b0	Master	Indicates that the write data is valid and can be read by the slave.
WREADY	1’b0	Slave	Indicates that the slave is ready to accept the write data.
WDATA	32’b0	Master	The data to be written to the address specified in the write address channel.
WSTRB	4’b0	Master	Write strobes, indicating which byte lanes are valid for writing (optional).

Table 3: Write Response Channel Signals.

Signal Name	Width	Source	Description
BVALID	1'b0	Slave	Indicates that the write response is valid and can be read by the master.
BREADY	1'b0	Master	Indicates that the master is ready to accept the write response.
BRESP	2'b0	Slave	Write response, indicating the status of the write transaction (e.g., OKAY, SLVERR).

Table 4: Read Address Channel Signals.

Signal Name	Width	Source	Description
ARVALID	1'b0	Master	Indicates that the address and control information are valid and can be read by the slave.
ARREADY	1'b0	Slave	Indicates that the slave is ready to accept the address and control information.
ARADDR	32'b0	Master	The read address from where data is to be read.

Table 5: Read Data Channel Signals.

Signal Name	Width	Source	Description
RVALID	1'b0	Slave	Indicates that the read data is valid and can be read by the master.
RREADY	1'b0	Master	Indicates that the master is ready to accept the read data.
RDATA	32'b0	Slave	The data read from the address specified in the read address channel.
RRESP	4'b0	Slave	Read response, indicating the status of the read transaction (e.g., OKAY, SLVERR).

LeWiz Communications, Inc.
1296 Kifer Road, #606
Sunnyvale, CA 94086 USA
info@LeWiz.com
www.LeWiz.com