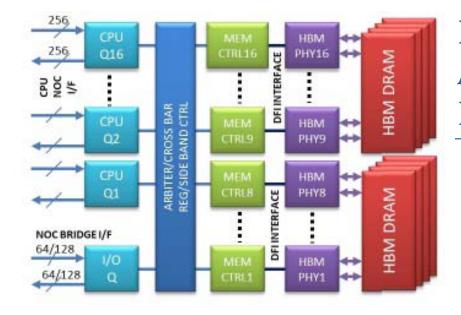# HBM Memory Controller IP Core

FAULT-TOLERANT AND HIGH BANDWIDTH

- **Multi-channel - data parallelism**
- **NOC or AXI-stream interface**
- **Support HBM devices**
- **Support DDR**
- **ECC, memory scrubbing, TMR**

Produced by DRAM manufacturers such as Samsung and Micron, **High Bandwidth Memory** or HBM, provides users with high bandwidth, low power consumption and large memory size. HBM is most commonly used in data intensive applications such as AI, image processing, vector processing and others. AI algorithms such as deep neural networks (DNN) store inputs and massive weight parameters, activations as the input traverses the neural network. DNN training requires large quantity of activation information to be stored and retrieved very quickly for multi-pass processing. A 50-layer ResNet network may require millions of weight parameters and millions of activations to be stored per pass. Floating point (and its precision level) further significantly increases the size of the memory by 100's of times. And for high performance, these different types of stored information must be fetched and fed into the neural network at high speed. Memory bandwidth is a major challenge in designing processing chips for data intensive applications. HBM helps to alleviate such problems. Chips such as **GPU**, application **accelerators**, **vector processors** require HBM controller to access the high bandwidth available from HBM. LeWiz offers HBM Controller IP core for designing ASIC and processing chips.

HBM is a JEDEC standard. It uses 3D stacking technology with through silicon vias to decrease the signal travel time (lowers the latency), increases memory density per area. Thus, HBM has smaller surface area and board space than other DRAM types. Due to its small surface area and high performance, HBM is a key integration for aerospace and commercial applications. HBM using the LeWiz HBM Controller can support error check and correction (ECC) with memory scrubbing capability – offering fault tolerant capability suitable for high-reliability and space applications. For radiation environment, space versions with different levels of tri-modular redundancy (TMR) are also available.

LeWiz HBM Controller has 16 parallel channels for data access. Each channel is 256-bit wide. In the backend it uses the DFI standard for interfacing to DRAM PHYs. In the front-end, it supports network-on-chip or standard, well-known bus AXI-stream for on-chip interface.

In addition to HBM, the IP core also supports DDRx DRAM types. Available in source code or netlist format. A test bench and the documents are also provides to help users in their application.

HBM Memory Controller

FEATURES:

- Low latency, high bandwidth
- Supports HBM or DDRx memory types
- 16 parallel access channels
- Multi, independent internal queues
- Bus width configurable from 64 bits to 256 bits
- Support large block data transfers (2048 bytes)
- Support DFI standard for DRAM PHY interfacing
- Low power mode and self-refresh
- TMR fault tolerant
- Hamming code ECC
- Memory scrubbing
- Supports multi-stack HBM configuration
- Advanced Peripheral Bus (APB) interface for core configuration

LeWiz Communications, Inc.
1296 Kifer Road, #606
Sunnyvale, CA 94086 USA
info@LeWiz.com
www.LeWiz.com