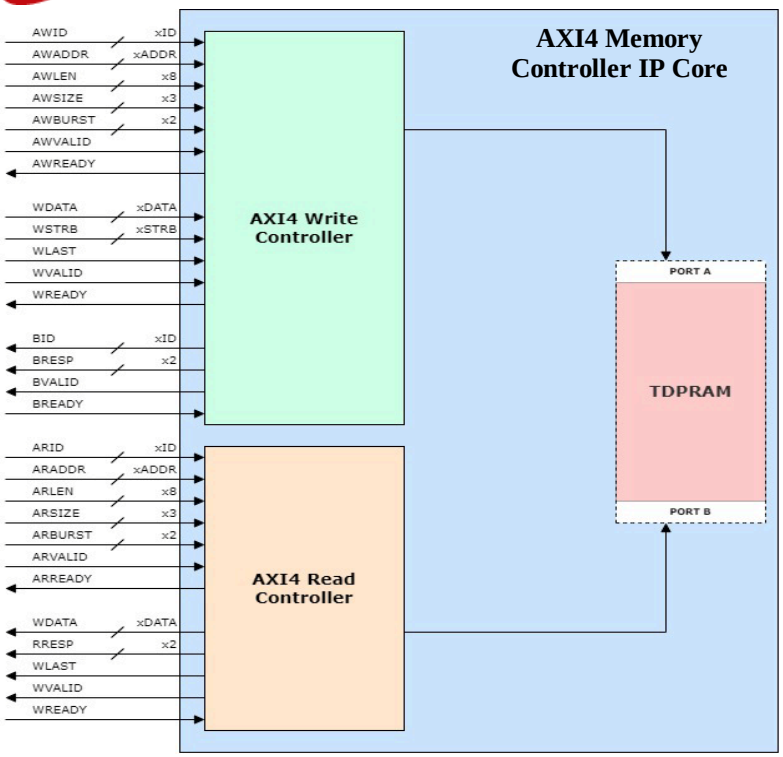
AXI4 Memory Controller IP Core



High Performance On-Chip Memory

- **Supports FIXED, INCR, and WRAP bursts**
- **Simultaneous Read/Write**
- **Optimize for throughput**
- **For program execution, data storage**
- **Memory-mapped addresses**

ASIC and SoC designs require on-chip memory for **on-chip program and data storage** to gain **high-performance** and **low power advantages**. To **reduce** risks, chip designs are usually emulated in **FPGA** hardware for thorough testing before taping out. Thus, on-chip memories use FPGA-like RAMs which are later replaced with silicon process' RAMs. LeWiz's AXI4 Memory Controller IP core enables the customer to emulate in FPGA and move ASIC designs to the silicon process seamlessly – 1 code flow from simulation, emulation to ASIC tape out; reducing risk of human errors.

Advanced eXtensible Interface 4 (AXI4) is widely used with **on-chip modules**. It allows for **ease of integration**, **greater bandwidth** with large data transfers (bursts) and **parallel read/write accesses** - supporting true dual-port RAM (**TDPRAM**). LeWiz IP core uses AXI4 bus for interfacing to customer's **internal bus**. It can be used with **RAMs** generated from the RAM compilers which may be available from the foundries or other providers. Applications for LeWiz AXI4 Memory Controller range from **microcontroller designs,** to **DSP chips**, to integrated **SoCs** for high performance systems and others.

The design of the AXI4 Memory Controller is tuned for **low latency**, **simultaneous** reads/writes, **efficient** bus cycle, **burst** accesses, and **fast** data transmission through **bidirectional** data transfers. It supports memory-mapped addressing – **simple** and **efficient** decoding.

FEATURES:

- Well known AXI4 protocol interface
- **Simultaneous** read/write accesses
- Supports burst data transmissions
- **FIXED, INCR, WRAP burst modes**
- Supports **narrow-lane, unaligned, unaligned narrow-burst transfers**
- Optimize for high performance, low power
- Can specify ID, Address, Data Bus width + TDPRAM depth
- Automatic AXI4 controller data width matches **TDPRAM**
- Automatic corresponding **AWSIZE/ARSIZE value** to bus width

AXI4 Memory Controller

AXI4 Signals

Signal	Bus Width	I/O	Description
ACLK	1	Input	Global clock signal.
ARESETn	1	Input	Global reset signal, active LOW.

Table 1: **AXI4 global signals**

Signal	Bus Width	I/O	Description
AWID	ID*	Input	Write address ID. Tag for the write address group.
AWADDR	ADDR*	Input	Write address. Address for the first transfer.
AWLEN	8	Input	Burst length. Indicates the number of beats/transfers within the upcoming burst (there are AWLEN +1 beats in a transfer).
AWSIZE	3	Input	Burst size for each transfer. Encoded; see official documentation.
AWBURST	2	Input	Burst type. Encoded signal indicating the type of burst. Valid inputs are: Fixed (b00), Incrementing (b01), & Wrapping (b10).
AWVALID	1	Input	Write address valid.
AWREADY	1	Output	Write address ready.

Table 2: **AXI4 Write Address channel busses**

Signal	Bus Width	I/O	Description
WDATA	DATA*	Input	Write data.
WSTRB	DATA* ÷ 8	Input	Write strobe. Each strobe bit indicates a byte of valid data.
WLAST	1	Input	Write last. Indicates final beat/transfer in a burst.
WVALID	1	Input	Write data valid.
WREADY	1	Output	Write data ready.

Table 3: **AXI4 Write Data channel busses**

Signal	Bus Width	I/O	Description
BID	ID*	Output	Write ID tag.
BRESP	2	Output	Write response. 2-bit Encoded signal indicating the transfer status: OKAY (b00), EXOKAY (b01), SLVERR (b10), DECERR(b11).
BVALID	1	Output	Write response valid.
BREADY	1	Input	Write response ready.

Table 4: **AXI4 write response channel signals**

Signal	Bus Width	I/O	Description
ARID	ID*	Input	Read address ID. Tag for the read address group.
ARADDR	ADDR*	Input	Read address. Address for the first transfer.
ARLEN	8	Input	Burst length. Indicates the number of beats/transfers within the upcoming burst (there are AWLEN +1 beats in a transfer).
ARSIZE	3	Input	Burst size for each transfer. Encoded; see official documentation.
ARBURST	2	Input	Burst type. Encoded signal indicating the type of burst. Valid inputs are: Fixed (b00), Incrementing (b01), & Wrapping (b10).
ARVALID	1	Input	Read address valid.
ARREADY	1	Output	Read address ready.

Table 5: **AXI4 Read Address channel busses**

Signal	Bus Width	I/O	Description
RID	ID*	Output	Read ID tag.
RDATA	DATA*	Output	Read data.
RRESP	2	Output	Read response. 2-bit Encoded signal indicating the transfer status: OKAY (b00), EXOKAY (b01), SLVERR (b10), DECERR(b11).
RLAST	1	Output	Read last. Indicates the final beat/transfer in a burst.
RVALID	1	Output	Read data valid.
RREADY	1	Input	Read data ready.

Table 6: **AXI4 Read Data channel busses**

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