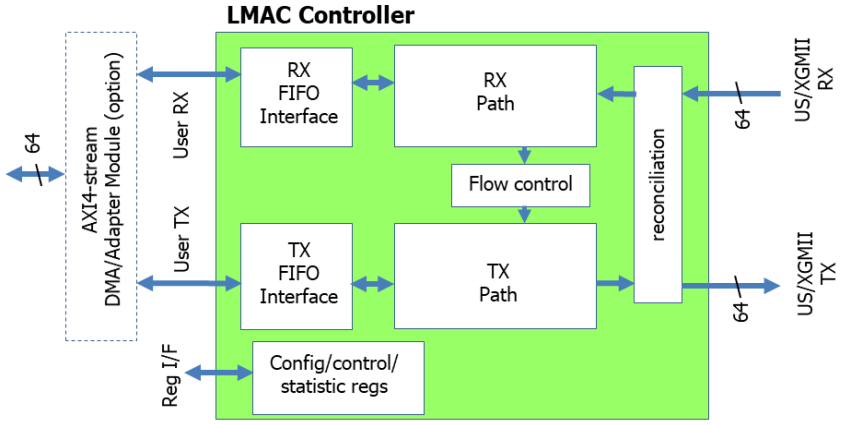
MAC-10G 1-10Gbps Ethernet MAC Controller



LeWiz provides a range of Ethernet MAC controllers from 100Gbps to 10Mbps for use in space, defense, and ultra-low latency applications. This datasheet is for the 10G/5G/2.5G/1Gbps Ethernet MAC IP core.

- Deployed extensively in production ranging from networking, video streaming, financial transaction, to computing and storage applications
- Designed to power up and work without software configuration
- Target for ASIC or FPGA deployment (support several Xilinx, Intel FPGA families)
- Available in source code

INTERFACES:

On the Ethernet side (right hand side of above diagram), the MAC interfaces directly to the serdes or PHY using standard XGMII interface for 10Gbps. It supports SGMII and other options for other speeds, e.g., 1G/2.5G/5G.

On the internal user logic side, it has 3 interfaces. Two are FIFO interfaces. One FIFO interface is used for transmit purposes (including data and control signals). The other is used for receiving purposes. A third interface is also available for interface to internal registers. This is the simple advanced peripheral bus interface standard (address, data, read/write control).

For **ultra-low latency** applications, a bond-out option can be provided to directly receive data from internal of the MAC by-passing other logics.

For **security applications**, a split interface option can be provided to enable the user to implement data filtering, deep packet inspection and other functions

For **space applications** (option), each core can be made available with built-in full or partial tri-modular redundancy

For AXI based internal bus system, an option can be provided to bond out as **AXI-stream interface** to the user. The design can be connected directly to DMA or smart, descriptor-based DMA functions (as shown above). FIFO interface and other interfaces in the MAC are 64-bit at 156MHz Ethernet clock rate. User clock or under internal bus can be designed to run at different clock (or much higher speed) than the MAC internal clock.

Sustain **full 10G line-rate** performance on both the receiving and transmitting side. Best performance even at smallest Ethernet packet size

FEATURES:

LeWiz MAC tracks the Ethernet line for link detection

On the receiving (RX) side, it:

- handles all Ethernet error conditions
- supports unicast, broadcast, multi-cast modes

- supports VLAN, ARP, PING, TCP/UDP, IP only, etc.
- checks the CRC
- checks for valid MAC address
- Supports jumbo frame (option)
- collects statistics (Many counters and flags) for debug
- collects error conditions
- (optional) RX TCP/UDP/IP checksum offload
- (optional) has the ability to classify packets to different types (based on IP, TCP info) to assist the user logic.
- (optional) RX side offload – receive side scaling to allow multi-core processing in parallel, more efficient system performance, power consumption at full 10G rate

On the transmit (TX) side, it:

- generates the CRC for the packet
- encapsulates the packet then
- interfaces with the SerDes/Ethernet side directly
- supports VLAN, ARP, PING,
- supports TCP/UDP, IP only, etc.
- collects statistics (Many counters and flags) for hardware/software debug
- (optional) TX checksum offload for TCP/UDP/IP
- (optional) supports TCP/UDP segmentation offload – large data block transmitting but still compatible with normal size Ethernet networks

If used in conjunction with LeWiz **smart, descriptor-based DMA** (option), the DMA uses command descriptors constructed by the device driver software to enable the MAC to transmit and receive without requiring CPU assistance. DMA will fetch data for the MAC on transmit and will place data into system memory for the software stack to process on receiving side. It features:

- AXI or AXI-stream interface
- Clock independent of MAC clock frequency
- Transmit based on descriptors, e.g., context, packet, packet header, packet payload descriptors
- RX descriptors for receiving side
- Support multi descriptor rings – each ring with a list of descriptors
- CPU offload for data handling
- OS flexibility with scatter gather (option)
- Capable of separate header and data descriptor
- Recycling of data buffers – efficient use of system memory
- Pre-load pack of buffers for high-speed transfer
- Multi-ring on RX for receive side scaling – CPU affinity (option)
- Direct load (user to hardware and vice versa for kernel by-pass) - option

Driver Support is available for Linux (Windows and others available based on customer request)

LeWiz also provides customization and design services to assist customers if required.

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