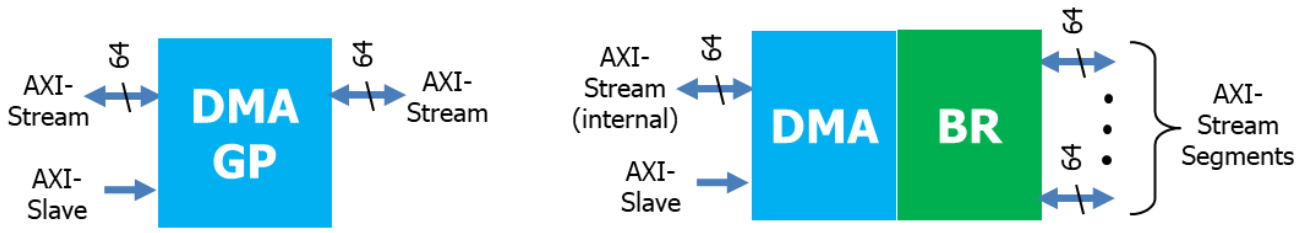
DMA-GP/BR General Purpose & Bridge DMA IP



LeWiz provides a range of direct memory access controllers (DMA) and bus bridge IP cores. These are **customizable** to user's SoC or design requirements. 3 classes of DMAs are offered:

- DMA-GP: DMA for general purpose applications (described in this datasheet)
- DMA-HP: Smart DMA for high performance applications such as high-speed Ethernet (See MAC-10G for description). This DMA makes the Ethernet interface looks more like a NIC device for Ethernet, thus much easier to work with for system development and offload CPU from handling Ethernet tasks for full bit rate performance.
- DMA-BR: DMA/Bus-Bridge combination to allow multiple peripherals or memory to connect to the SoC internal bus or complex PCI-express bus.

This datasheet describes the general-purpose DMA controller and the DMA Bridge IP cores.

DMA-GP Core (left of the above figure)

The DMA-GP core moves data between a source and a destination such as between memory and I/O peripheral device (or vice versa). Data moved can be small or large data block. Each move is controlled by the host software with simple register configuration of source/destination addresses, size of data, and control.

Features:

- AXI/AXI4 compliant
- Optional Scatter/Gather Direct Memory Access (DMA)
- AXI/AXI4 data width support of 32, 64, 128, 256
- Programmable source/destination address – up to 64-bit addressing
- Programmable transfer size, enable/disable control
- Programmable bus burst length – number of data beats per burst
- Optional Data Re-Alignment support
- Supports interrupt or software polling
- Optional queuing support for task list – for CPU offload
- Supports any endian mode
- Available in Verilog source, test bench (optional)
- Optional software driver for Linux or other OS

DMA-BR Core (Right of the above figure)

DMA-BR offers similar capability to move data between different devices such as system memory to peripherals and vice versa. It also incorporates a bridge between the host (internal bus) and multiple peripherals (see figure above). This allows multiple peripherals to share DMA channel(s) on one internal bus segment.

Useful for grouping multiple peripherals together with a DMA-Bridge to form a single module in the SoC. Data can be DMA-ed from a peripheral (in the module) to the internal bus memory (or vice versa), for example. Or data can be DMA-ed between the peripherals.

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